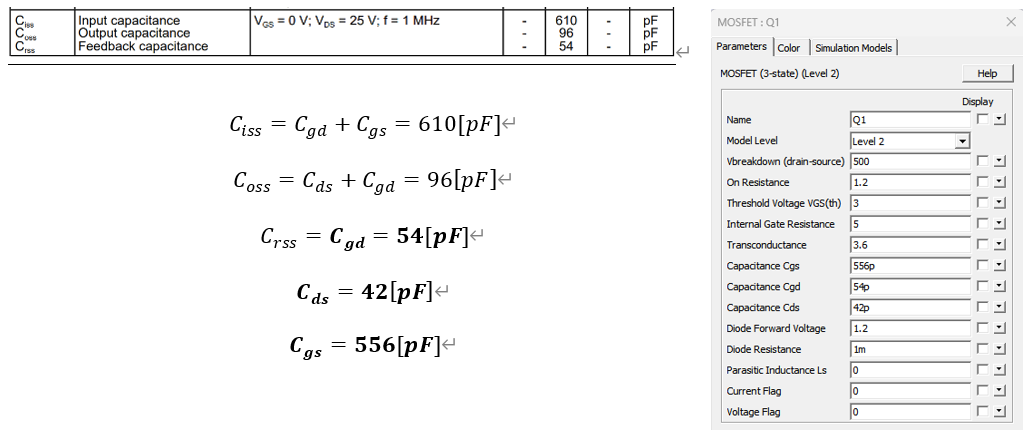
***LAB1 HW***

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*Question 1*, show how operation of MOSFET would be effected by Cgd, and Cds by drawing curves of VDS [V] and ID [A]. Please, compare it with ideal MOSFET operation and consider explain it with Miller Plateau. Feel free to give an example to answer the question.

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**Figure 1.

테이블이(가) 표시된 사진

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자동 생성된 설명Figure 2. Practical MOSFET Firing Circuit

Figure 3. Ideal and Practical MOSFET Operation

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Figure 4. Practical MOSFET Circuit with sources

Figure 3 shows that the curves of the and graphs rise vertically in the IDEAL model, while the curves of the and graphs in the PRACTICAL model maintain constant values during increase or decrease.

By the parasitic capacitance Cgd, Cgs, and Cds, it can be seen that the PRACTICAL MODEL exhibits a different graph curve from the IDEAL model.

In Question 2, explain why those Op-Amps are connected in between two voltage dividers. Please, explain it with ideal equivalent circuit of an Op-Amp.

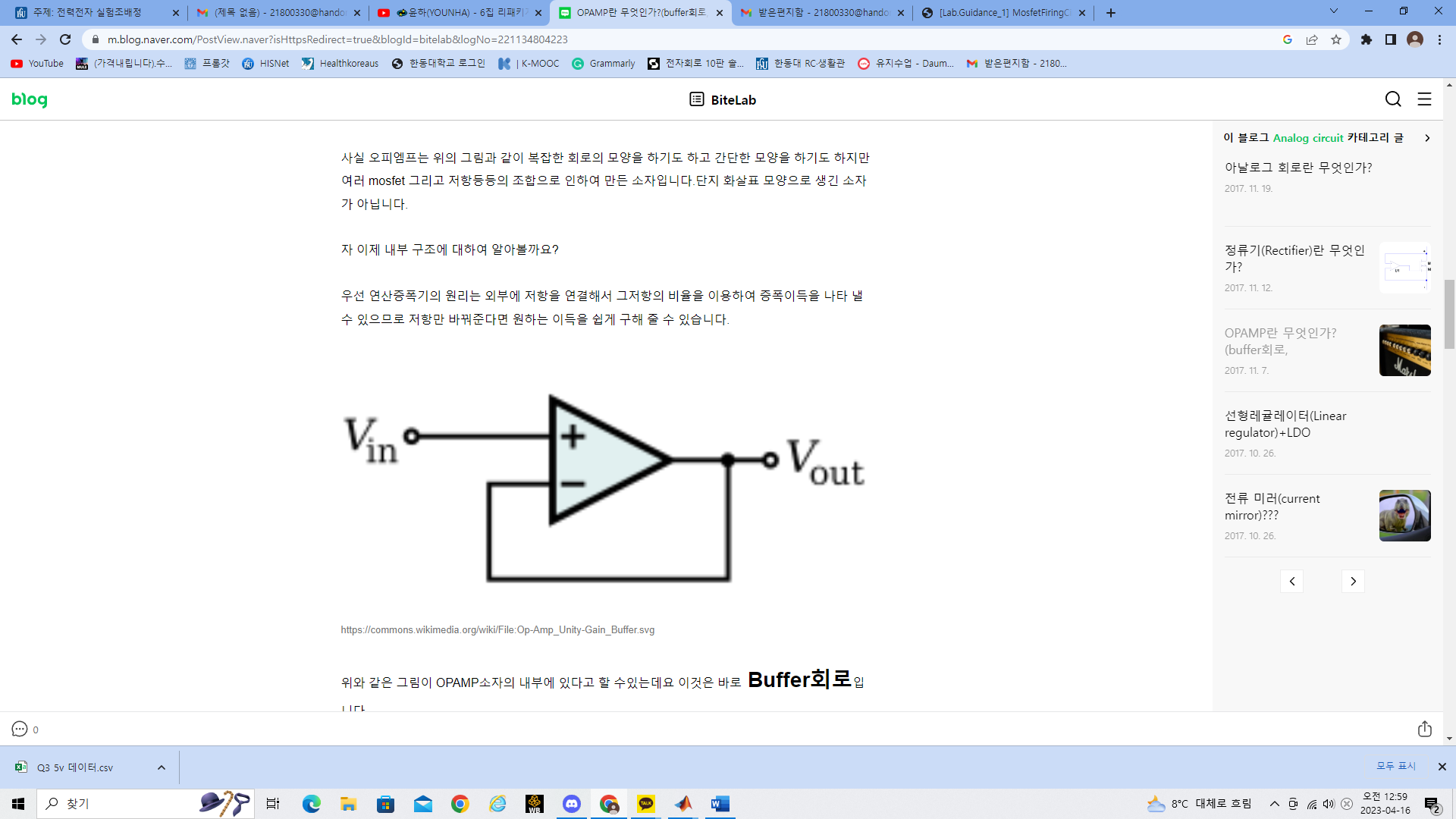


Figure 5. Circuit of Buffer OP-AMP

Figure 5 show the circuit of buffer op-amp and we know that buffer’s gain is 1. This means Input and Output is same. Buffer to prevent delay of the signal. When we transmit a signal, noise is easily generated when the impedance is high. In that case, since the signal B should not come when we send A, it is a way to reduce the impact of external noise by lowering the impedance. Buffers have infinite input impedance and small output impedance, so we use buffer to reduce the noise of signal.

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Figure 6. Structure of Dual OP-AMP

In MFC, we use Dual OP-AMP that combine with two Buffer op-amp. It is considered that it was used to minimize noise generation by reducing input impedance using two buffer circuits.

In Question 3, draw curves of Vgs vs time when Vg = 5[V] and Vg = 12[V] in MATLAB for comparison. See, how fast they reach to 4[V] of threshold voltage.



Figure7. Vgs vs time when Vg = 5[V] and Vg = 12[V]

In Figure 7, we can see the graph of Vgs(= output of Gate Driver) and Vg(input Voltage). Yellow line is the graph when Vg = 12V, and purple line is the graph when Vg= 5v. Now see the Figure 8.

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Figure 8. Expansion of Figure7

Figure 8 is expansion of Figure 7. In MFC, Mosfet(IRF 830)’s Threshold voltage is 4[v]. We can see Vg=12v reach first at Vth in comparison with Vg=5v. AS a result when Vg is 12v, the Threshold Voltage is reached faster, and the MOSFET’s operating point occur faster.



Figure 9. Vgs and Vds in MOSFET operation

Figure 9 is the graph when MOSFET’s switch operation. The voltage applied from the PWM enters the gate of the MOSFET, at which time the switch operation of the MOSFET occurs. When the switch is off, the current flowing to the gate stops and the voltage applied to the drain is trapped. Therefore, when looking at the waveform, the two voltages appear in an inverted phase.